Listing of Claims:

Claim 1 (original): A system comprising:

a controller responsive to interrupt signals received on one or more interrupt signal inputs;

an interrupt message receiver coupled to the one or more interrupt signal inputs; and

a plurality of interrupt sources to transmit interrupt messages to the interrupt message receiver through a data bus,

wherein the interrupt message receiver further comprises logic to initiate interrupt signals on the one or more interrupt signal inputs in response to receipt of interrupt messages from the data bus.

Claim 2 (original): The system of claim 1, wherein the interrupt message receiver comprises logic to decode each interrupt message in response to receipt of one or more write transactions received from the data bus.

Claim 3 (original): The system of claim 1, wherein the system further comprises a register of bits, each interrupt source corresponding with one bit, and wherein the interrupt message receiver comprises logic to set a bit in response to receipt of an interrupt message from an interrupt source corresponding with the bit and wherein the controller comprises logic to clear the bit in response to completion of servicing an interrupt associated with the interrupt message.

Claim 4 (original): The system of claim 1, wherein the controller comprises a first interrupt signal input to receive an IRQ interrupt signal and a second interrupt signal input to receive a FIQ interrupt signal.

Claim 5 (original): The system of claim 1, wherein controller comprises logic to service interrupts in response to interrupt signals received on the one or more interrupt signal inputs the system further comprises an interrupt controller comprising:

logic to maintain a record of at least one unserviced interrupt message received at the interrupt message receiver from an interrupt source; and

logic to initiate an interrupt signal on an interrupt signal input in to service the unserviced interrupt message in response to completion of an interrupt service by the controller.

Claim 6 (original): The system of claim 5, wherein the interrupt controller further comprises:

logic to define a priority for one or more interrupt sources;

logic to maintain a queue of unserviced interrupt messages based upon the priority; and

logic to select an unserviced interrupt message from the queue in response to completion of an interrupt service by the controller.

Claim 7 (original): The system of claim 5, wherein the interrupt controller further comprises a plurality of interrupt signal inputs and the interrupt controller further comprises:

logic to associate each interrupt source with an interrupt signal input;

logic to maintain a queue of unserviced interrupt messages for each interrupt signal input, each unserviced interrupt messages being received from an interrupt source associated with the interrupt signal input; and

logic to select an unserviced interrupt message from a queue in response to completion of an interrupt service initiated at the interrupt signal input associated with the queue.

Claim 8 (original): The system of claim 1, wherein the system comprises a plurality of controllers, each controller comprising one or more interrupt signal inputs, and wherein the interrupt message receiver is coupled to each interrupt signal input of the controllers.

Claim 9 (original): A method comprising:

receiving interrupt messages on a data bus from a plurality of interrupt sources; and

selectively initiating interrupt signals to a controller on one or more interrupt signal inputs in response to each received interrupt message.

Claim 10 (original): The method of claim 9, wherein the method further comprises decoding each received interrupt message in response to receipt of one or more write transactions received from the data bus.

Claim 11 (original): The method of claim 9, wherein the method further comprises:

setting a bit in a register of bits in response to receipt of an interrupt message from an interrupt source corresponding with the bit, each interrupt source corresponding with one bit in the register; and

clearing the bit in response to completion of servicing an interrupt associated with the interrupt message.

Claim 12 (original): The method of claim 9, wherein the method further comprises selectively initiating interrupt signals to a controller on a first interrupt signal input corresponding with an IRQ interrupt signal and on a second interrupt signal input corresponding with a FIQ interrupt signal.

Claim 13 (original): The method of claim 9, wherein method further comprises:

maintaining a record of at least one unserviced interrupt message received at the interrupt message receiver from an interrupt source; and

initiating an interrupt signal on an interrupt signal input to service the unserviced interrupt message in response to completion of an interrupt service by the controller.

Claim 14 (original): The method of claim 9, the method further comprising:

defining a priority for one or more interrupt sources;

maintaining a queue of unserviced interrupt messages based upon the priority; and

selecting an unserviced interrupt message from the queue in response to completion of an interrupt service by the controller.

Claim 15 (original): The method of claim 14, wherein the method further comprises:

associating each interrupt source of with one of a plurality of interrupt signal inputs;

maintaining a queue of unserviced interrupt messages for each interrupt signal input, each unserviced interrupt messages being received from an interrupt source associated with the interrupt signal input; and

selecting an unserviced interrupt message from a queue in response to completion of an interrupt service initiated at the interrupt signal input associated with the queue.

Claim 16 (original): An interrupt message receiver comprising:

an interface to a data bus to receive interrupt messages from a plurality of interrupt sources; and

logic to initiate interrupt signals to a controller on interrupt signal inputs in response to receipt of the interrupt messages.

Claim 17 (original): The interrupt message receiver of claim 16, wherein the interrupt message receiver comprises logic to decode each interrupt message in response to receipt of one or more write transactions received from the data bus.

Claim 18 (original): The interrupt message receiver of claim 16, wherein the interrupt message receiver further comprises:

logic to set a bit in a register of bits in response to receipt of an interrupt message from an interrupt source corresponding with the bit; and

logic to clear the bit in response to completion of servicing an interrupt associated with the interrupt message.

Claim 19 (original): The interrupt message receiver of claim 16, the interrupt message receiver further comprising:

logic to transmit interrupt signals on a first interrupt signal input to provide an IRQ interrupt signal; and

logic to transmit interrupt signals on a second interrupt signal input to provide an FIQ interrupt signal.

Claim 20 (original): The interrupt message receiver of claim 16, wherein the interrupt message receiver further comprises an interrupt controller comprising:

logic to maintain a record of at least one unserviced interrupt message received from an interrupt source; and

logic to initiate an interrupt signal on an interrupt input signal to service the unserviced interrupt message in response to completion of an interrupt service.

Claim 21 (original): The interrupt message receiver of claim 20, wherein the interrupt controller further comprises:

logic to define a priority for one or more interrupt sources;

logic to maintain a queue of unserviced interrupt messages based upon the priority; and

logic to select an unserviced interrupt message from the queue in response to completion of an interrupt service.

Claim 22 (original): The interrupt message receiver of claim 20, wherein the interrupt controller further comprises:

logic to associate each interrupt source with an interrupt signal input;

logic to maintain a queue of unserviced interrupt messages for each interrupt signal input, each unserviced interrupt messages being received from an interrupt source associated with the interrupt signal input; and

logic to select an unserviced interrupt message from a queue in response to completion of an interrupt service initiated at the interrupt signal input associated with the queue.

Claim 23 (original): An apparatus comprising:

means for receiving interrupt messages on a data bus from a plurality of interrupt sources; and

means for selectively initiating interrupt signals to a controller on one or more interrupt signal inputs in response to each received interrupt message.

Claim 24 (original): The apparatus of claim 23, wherein the apparatus further comprises means for decoding each received interrupt message in response to receipt of one or more write transactions received from the data bus.

Claim 25 (original): The apparatus of claim 23, wherein the apparatus further comprises:

means for setting a bit in a register of bits in response to receipt of an interrupt message from an interrupt source corresponding with the bit, each interrupt source corresponding with one bit in the register; and

means for clearing the bit in response to completion of servicing an interrupt associated with the interrupt message.

Claim 26 (original): The apparatus of claim 23, wherein the apparatus further comprises means for selectively initiating interrupt signals to a controller on a first interrupt signal input corresponding with an IRQ interrupt signal and on a second interrupt signal input corresponding with a FIQ interrupt signal.

Claim 27 (original): The apparatus of claim 23, wherein apparatus further comprises:

means for maintaining a record of at least one unserviced interrupt message received at the interrupt message receiver from an interrupt source; and

means for initiating an interrupt signal on an interrupt signal input to service the unserviced interrupt message in response to completion of an interrupt service by the controller.

Claim 28 (original): The apparatus of claim 23, the apparatus further comprising:

means for defining a priority for one or more interrupt sources;

means for maintaining a queue of unserviced interrupt messages based upon the priority; and

means for selecting an unserviced interrupt message from the queue in response to completion of an interrupt service by the controller.

Claim 29 (original): The apparatus of claim 28, wherein the apparatus further comprises:

means for associating each interrupt source of with one of a plurality of interrupt signal inputs;

means for maintaining a queue of unserviced interrupt messages for each interrupt signal input, each unserviced interrupt messages being received from an interrupt source associated with the interrupt signal input; and

means for selecting an unserviced interrupt message from a queue in response to completion of an interrupt service initiated at the interrupt signal input associated with the queue.